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APPLICATION FOR LETTERS PATENT OF THE UNITED STATES

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TITLE OF INVENTION:

Zero Static Power Fuse Cell For Integrated Circuits

TO WHOM IT MAY CONCERN, THE FOLLOWING IS
A SPECIFICATION OF THE AFORESAID INVENTION

ZERO STATIC POWER FUSE CELL FOR INTEGRATED CIRCUITS

Field of the Invention

The present invention relates generally to integrated circuits (ICs). More particularly, the invention relates to fuses used in ICs.

Background of the Invention

Fuse cells are widely used in integrated circuits. As an example, fuse cells can be used to store addressing information of defective memory cells in an array for redundancy applications. Fig. 1 shows a conventional fuse cell 101 comprising a pull-up circuit. As shown, a fuse 110 is coupled between the pull-up (logic 1 or high) power source and ground (logic 0 or low). Coupled between the fuse and the pull-up power source is a fuse cell output terminal 160. The output signal of the fuse cell indicates the state of the fuse (cut or uncut). A cut fuse produces a logic 1 output while an uncut fuse produces a logic 0 output.

When the fuse is not cut, the pull-up power source is coupled to ground via the fuse. Thus, even when the fuse is in a static state, power dissipates through the

fuse which increases the IC's power consumption. The increased power consumption is undesirable, particularly for low power applications.

As evidenced from the above discussion, it is desirable to provide an improved fuse cell with reduced or no static power dissipation.

Summary of the Invention

The invention relates generally to fuse cells. In particular, the invention relates to a fuse cell having reduced or no static power consumption. In one embodiment, the fuse cell includes a control circuit, a fuse circuit, an initialization circuit and a latch. The control circuit is coupled to the latch, fuse circuit and initialization circuit. In response to an active initialization signal, the control circuit couples the latch to the initialization circuit. The initialization circuit sets the latch to a first state. After fuse cell is initialized, the initialization signal is deactivated which causes the fuse cell to operate in the normal operating mode. In the normal operating mode, the initialization circuit is decoupled from the latch while the fuse circuit is coupled to the latch. Depending on the fuse state, the latch remains

in the first state or is switched to a second logic state.

Brief Description of the Drawings

Fig. 1 shows a conventional fuse cell; and

Figs. 2-6 show fuse cells in accordance with various embodiments of the invention.

Preferred Embodiments of the Invention

Fig. 2 shows a block diagram of a fuse cell 201 having reduced or no static power dissipation. In accordance with the invention, static power dissipation is avoided or reduced by using a latch 240, which is coupled to a fuse 210, to store or generate information related to the state of the fuse. The information is provided at a fuse cell output terminal 160 coupled to the latch. A control circuit 270 is coupled to the fuse and the latch. The control circuit includes an input terminal 265 for receiving a fuse reset or control signal to initialize the fuse.

To initialize the fuse cell, an active init signal is provided at the input terminal. In one embodiment, the active init signal comprises an active low (logic 0) signal. The init signal, for example, can be the power on reset signal. During initialization, the latch is

decoupled from the fuse and set to a known state or logic level (first state). The init signal is then inactivated (e.g., logic 1) after initialization is completed. Inactivating the init signal couples the latch to the fuse. Depending on the whether the fuse is cut or uncut, the latch remains at the first state or is flipped to the second state.

In one embodiment, the latch is initialized to store a logic 1, producing a logic 1 output. A cut fuse does not affect the state of the latch (or the fuse cell output) while an uncut fuse causes the latch state to switch from a logic 1 to a logic 0. The switch in logic level in the case of an uncut fuse is due to the fact that the fuse is coupled to ground. By using the latch, the present invention avoids having a pull-up power source being connected to ground when the fuse is uncut, as in the case of conventional fuse cell, thereby reducing or eliminating static power dissipation.

Referring to Fig. 3, a fuse cell in accordance with one embodiment of the invention is shown. The fuse cell comprises a control circuit 270, a latch 240, an initialization circuit 225, and a fuse circuit 210. The latch includes first and second terminals 341 and 342 which are commonly coupled to first and second inverters

345 and 346 back-to-back. The first and second latch terminals are coupled to output terminals 367 and 368 of the control circuit.

In one embodiment, the control comprises first and second transistors 330 and 335. The transistors, for example, are n-FETs. First and second terminals of the first transistor are coupled to the first terminal of the latch and the initialization circuit. In one embodiment, the initialization circuit comprises a pull-down power source such as ground. The second transistor's first and second terminals are coupled to the second terminal of the latch and the fuse circuit. In one embodiment, the fuse circuit comprises a fuse 110 coupled to ground 106. The gates of the transistors are coupled to the input terminal of the control circuit or through an inverter. The first and second transistors operate in a push-pull configuration. That is, one transistor is on (conductive) while the other is off (non-conductive). In one embodiment, an inverter 375 is located between the input terminal and the first transistor, causing the n-FETs to operate in a push-pull configuration.

The fuse cell is initialized by providing an active low input signal. The active low signal switches the

first transistor on and the second transistor off, coupling the first terminal of the latch to the initialization circuit and decoupling the second terminal of the latch from the fuse circuit. This causes the latch to be initialized to a logic 1 state (i.e., first latch terminal is low while the second latch terminal is high). After the latch is initialized, the input signal is inactivated (logic 1) to decouple the first terminal of the latch from ground and to couple the second terminal of the latch to the fuse circuit. If the fuse is cut, the latch remains unchanged. An uncut fuse causes the second terminal of the latch to be coupled to ground via the fuse, switching the state of the latch from a logic 1 to a logic 0.

In one embodiment, an output stage 380 is coupled between the second terminal of the latch and fuse cell output terminal. The output stage comprises a capacitor 385 coupled between the output terminal and ground. In an alternative embodiment, as shown in Fig. 4, the output stage 480 comprises a CMOS capacitor 485 such as a p-FET. The capacitor serves to stabilize the fuse cell output from glitches. An inverter 382 may

optionally be provided to switch the logic of the fuse cell output signal.

Fig. 5 shows a fuse cell in accordance with another embodiment of the invention. The fuse cell, as shown, provides a valid fuse state during initialization. This is particularly useful for applications which require a valid fuse output during power-up (e.g., power supply under-voltage detection applications). The fuse cell comprises a latch 540, a control circuit 270, an initialization circuit 225, and a fuse circuit 210. To enable a valid fuse output signal even during power up, the control circuit couples the fuse to the latch at least from the time the IC is powered up. This enables a valid fuse cell output even during initialization. A resistor 546 is provided between the output of the first latch inverter and power source 106 of the fuse to reduce power dissipation during initialization if the fuse is uncut. Alternatively, a transistor 646, such as a p-FET, as shown in Fig. 6 can serve as a resistive element.

In one embodiment, the latch includes first and second terminals 341 and 342 which are commonly coupled to first and second inverters 345 and 346 back-to-back. A resistor 546 is also commonly coupled to the inverters

(e.g., output terminal of the first inverter and input terminal of the second inverter) and the second latch terminal.

The first and second latch terminals are coupled to output terminals 367 and 368 of the control circuit. The control circuit comprises first and second transistors 330 and 335. The transistors, for example, are n-FETs. First and second terminals of the first transistor are coupled to the first terminal of the latch and the initialization circuit. The second transistor's first and second terminals are coupled to the second terminal of the latch and the fuse circuit.

The first transistor and the second inverter of the latch operate in a push-pull configuration. That is, when one is on, the other is off. In one embodiment, the second latch inverter and the first transistor are controlled by the input signal at the input terminal 265 of the control circuit (init signal). In one embodiment, the second inverter is coupled to the input terminal while an inverter 375 is located between the input terminal and the gate of the first transistor, causing the first transistor and the inverter to operate in a push-pull configuration. The second transistor is

controlled by inverted input signal, which is used to control the first transistor.

The fuse cell is initialized by providing an active low input signal, for example, an init signal during power up. The active low signal switches the first transistor on and the second inverter off, coupling the first terminal of the latch to the logic 0 power source. At the same time, an active signal (logic 1) is provided at input terminal 266 to switch on the second transistor in order to couple the latch to the fuse. By switching off the second inverter during initialization, the second terminal 342 is decoupled from the first terminal 341 to avoid conflict between the first and second latch terminals caused by an uncut fuse.

The logic 0 power source causes the latch to produce a logic 1 signal at the output of inverter 345. Since the fuse is coupled to this point via the resistor, a valid fuse cell output is provided at the second terminal 342 during initialization. If the fuse is cut, the fuse output is a logic 1, otherwise the fuse output is a logic 0.

After initialization phase is completed, the init signal is inactivated while the control signal at input terminal 266 remains active. This decouples the logic 0

power source from the latch and activates the second inverter. An optional output stage, as described in Figs. 3 and 4, may be provided between the second terminal of the latch and the fuse cell output terminal. Alternatively, as shown in Fig. 5, one terminal of capacitor 585 of the output stage 580 is commonly coupled to the resistor and first inverter of the latch while the other terminal is coupled to ground.

While the invention has been particularly shown and described with reference to various embodiments, it will be recognized by those skilled in the art that modifications and changes may be made to the present invention without departing from the spirit and scope thereof. The scope of the invention should therefore be determined not with reference to the above description but with reference to the appended claims along with their full scope of equivalents.